Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-14. (Cancelled)

15. (Cancelled)

16. (Currently amended) The method of claim [[15]] 26 wherein planarized portions of the conformal layer located between opposing isolation structures at least partially form a memory device.

17. (Currently amended) The method of claim [[15]] 16 wherein the memory device is a floating gate field effect transistor device.

18. (Currently amended) The method of claim [[15]] 26 wherein the transistors formed in the voids include MOSFETs.

19. (Currently amended) The method of claim [[15]] 26 wherein the substrate is selected from the group consisting of:

a silicon containing substrate;

a silicon-on-insulator (SOI) substrate;

a germanium epitaxial layer on a silicon substrate;

a germanium epitaxial layer on a sapphire substrate;

a silicon on nothing (SON) substrate:

a plastic substrate; and

a flexible substrate.

20. (Currently amended) The method of claim [[15]] 26 wherein the protective layer comprises a dielectric material having a dielectric constant ranging between about 5.5 and about 9.

21. (Currently amended) The method of claim [[15]] 26 wherein the protective layer comprises a nitrogen containing layer.

22. (Currently amended) The method of claim [[15]] 26 wherein the protective layer comprises an oxygen containing layer.

23. (Currently amended) The method of claim [[15]] 26 wherein the conformal layer comprises a gate electrode layer.

24. (Original) The method of claim 23 wherein the gate electrode layer has a thickness ranging between about 300 angstroms and about 2000 angstroms.

25. (Original) The method of claim 23 wherein the gate electrode layer comprises a silicon containing layer formed by an LPCVD process.

26. (Previously presented) A method of manufacturing a microelectronic device, comprising:

providing a substrate having a protective layer located thereon and a plurality of isolation structures extending through the protective layer and at least partially into the substrate;

forming a mask over a first portion of a surface collectively formed by the protective layer and the plurality of isolation structures, the masked first portion thereby sharing a boundary with an unmasked second portion of the surface;

removing sacrificial portions of the protective layer from within the unmasked second portion;

removing the mask;

forming a conformal layer over remaining portions of the protective layer, the isolation structures, and in voids created by the removal of the sacrificial portions of the protective layer;

planarizing the conformal layer such that the conformal layer, the isolation structures, and the remaining portions of the protective layer are substantially coplanar;

removing the remaining portions of the protective layer; and

forming transistors in voids created by the removal of the remaining portions of the protective layer;

wherein planarizing the conformal layer comprises planarizing by at least one of a chemical mechanical polishing (CMP) process and an etching process.

27. (Currently amended) The method of claim [[15]] 26 further comprising forming a recessed portion of the conformal layer after planarizing the conformal layer.

28. (Original) A method of manufacturing a microelectronic device, comprising:

providing a substrate having a protective layer located thereon and a plurality of isolation structures extending through the protective layer and at least partially into the substrate, the substrate including at least one memory cell region and at least one periphery region;

forming a mask over a at least a portion of the periphery region and exposing at least a portion of the memory cell region;

removing sacrificial portions of the protective layer from within the memory cell region;

removing the mask;

forming a conformal layer over remaining portions of the protective layer, the isolation structures, and in voids created by the removal of the sacrificial portions of the protective layer;

planarizing the conformal layer such that the conformal layer, the isolation structures, and the remaining portions of the protective layer are substantially coplanar;

removing the remaining portions of the protective layer; and

forming transistors in voids created by the removal of the remaining portions of the protective layer.

29. (Original) The method of claim 28 wherein the memory device is a floating gate field effect transistor device.

30. (Previously presented) A method of manufacturing a microelectronic device, comprising:

providing a substrate having a protective layer located thereon and a plurality of isolation structures extending through the protective layer and at least partially into the substrate, the substrate including at least one memory cell region and at least one periphery region;

forming a mask over a at least a portion of the periphery region and exposing at least a portion of the memory cell region;

removing sacrificial portions of the protective layer from within the memory cell region;

removing the mask;

forming a conformal layer over remaining portions of the protective layer, the isolation structures, and in voids created by the removal of the sacrificial portions of the protective layer;

planarizing the conformal layer such that the conformal layer, the isolation structures, and the remaining portions of the protective layer are substantially coplanar;

removing the remaining portions of the protective layer; and

forming transistors in voids created by the removal of the remaining portions of the protective layer, wherein the transistors formed in the voids include MOSFETs.

31. (Original) The method of claim 28 wherein the substrate is selected from the group consisting of:

a silicon containing substrate;

a silicon-on-insulator (SOI) substrate;

a germanium epitaxial layer on a silicon substrate;

a germanium epitaxial layer on a sapphire substrate;

a silicon on nothing (SON) substrate;

a plastic substrate; and

a flexible substrate.

32. (Original) The method of claim 28 wherein the protective layer comprises a dielectric material having a dielectric constant ranging between about 5.5 and about 9.

33. (Original) The method of claim 28 wherein the protective layer comprises a nitrogen containing layer.

34. (Original) The method of claim 28 wherein the protective layer comprises an oxygen containing layer.

35. (Original) The method of claim 28 wherein the conformal layer comprises a gate electrode layer.

36. (Original) The method of claim 35 wherein the gate electrode layer has a thickness ranging between about 300 angstroms and about 2000 angstroms.

37. (Original) The method of claim 28 wherein the gate electrode layer comprises a silicon containing layer formed by a LPCVD process.

38. (Original) The method of claim 28 wherein planarizing the conformal layer comprises planarizing by at least one of a chemical mechanical polishing (CMP) process and an etching process.

39. (Original) The method of claim 28 further comprising forming a recessed portion of the conformal layer after planarizing the conformal layer.

40-48. (Cancelled)